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CLAIMS:

What is claimed is:

1. An interface for interconnecting electronic components, comprising:

at least one single-ended data signal;

a differential data signal pair;

a receiver for detecting said single-ended data signal, wherein detection of said single-ended data signal is made in conformity with a common mode voltage of said differential data signal pair.

2. The interface of Claim 1, wherein said receiver comprises:

a differential comparator coupled to said differential data signal pair; and

a singlential comparator coupled to said differential comparator and further coupled to said differential data signal pair and said single-ended data signal.

3. The interface of Claim 2, wherein said singlential comparator sums a non-inverted signal of said differential data signal pair and an inverted signal of said differential data signal pair to provide a reference for detecting said single-ended data signal.

4. The interface of Claim 2, wherein said singlential comparator comprises means for summing a non-inverted signal of said differential data signal pair and an inverted signal of said differential data signal pair to provide a reference for detecting said single-ended data signal.

5. The interface of Claim 3, wherein said singlential comparator comprises:

a first transistor having a gate coupled to said single-ended data signal ;

a second transistor having a gate coupled to a non-inverted signal of said differential data signal pair;

a third transistor having a gate coupled to an inverted signal of said differential data signal pair; and

a current source coupled to a channel connection of said first transistor, a channel connection of said second transistor and a channel connection of said third transistor, whereby said singlential comparator detects a difference between said single-ended data signal and an average of said non-inverted signal and said inverted signal of said differential data signal pair.

6. The interface of Claim 5, wherein said differential comparator comprises:

a fourth transistor having a gate coupled to said non-inverted signal of said differential data signal pair; and

a fifth transistor having a gate coupled to said inverted signal of said differential data signal pair and a first channel connection coupled to a resistor for providing active mode operation; and

a current source coupled to a channel connection of said fourth transistor and a second channel connection of said fifth transistor, whereby said differential comparator detects a difference between said said non-inverted signal and said inverted signal of said differential data signal pair, and wherein a gain of said active mode of said differential comparator is equal to a a gain of said singlential comparator.

7. The interface of Claim 2, wherein said receiver further comprises a multiplexer for producing a data output signal corresponding to said single-ended data signal, having a first input coupled to an output of said differential comparator, a second input coupled to an inverted output of said differential comparator, and a select input coupled to said output of said differential comparator and an output of said singlential comparator such that said output of said differential comparator is selected when said single-ended signal is at an equal logic value with said differential data signal pair and wherein said inverted output of said differential comparator is selected when said single-ended signal and said differential data signal pair are at unequal logic levels.

8. The interface of Claim 7, wherein said receiver further comprises:

a first latch for coupling said differential comparator to said multiplexer, said first latch having an input coupled to said output of said differential comparator and an output coupled to said first input of said multiplexer;

an inverter having an input coupled to said output of said first latch for producing said inverted output of said differential comparator and having an output coupled to said multiplexer;

a second latch for latching said output of said singlential comparator; and

an exclusive-OR gate having a first input coupled to said output of said first latch and a second input coupled to an output of said second latch and an output coupled to a select input of said multiplexer for selecting said output of said first latch when said single-ended signal is at an equal logic value with said differential signal pair and for selecting said output of said inverter when said single-ended signal and said differential data signal pair are at unequal logic levels.

9. The interface of Claim 1, wherein said receiver comprises:

a first differential comparator coupled to said differential data signal pair;

a second differential comparator coupled to a non-inverted signal of said differential signal pair and said single ended-data signal;

a third differential comparator coupled to an inverted signal of said differential signal pair and said single ended data signal; and

means for selecting between an output of said second differential comparator and an output of said third differential comparator to produce a data output corresponding to a logic value of said single-ended data signal.

10. The interface of Claim 1, wherein said receiver comprises:

a first differential comparator coupled to said differential data signal pair;

a second differential comparator coupled to a non-inverted signal of said differential signal pair and said single ended-data signal;

a third differential comparator coupled to an inverted signal of said differential signal pair and said single ended data signal; and

a logic circuit coupled to said first differential comparator, said second differential comparator and said third differential comparator for selecting between an output of said second differential comparator and said third differential comparator to produce a data output corresponding to a logic value of said single-ended data signal.

11. The interface of Claim 10, wherein said logic circuit comprises:

a multiplexer for producing said data output corresponding to said logic value of said single-ended data signal;

a first latch having an input coupled to an output of said first differential comparator;

a second latch having an input coupled to an output of said second differential comparator and an output coupled to a first input of said multiplexer;

a third latch having an input coupled to an output of said third differential comparator and an output coupled to a second input of said multiplexer;

a first exclusive-OR gate having inputs coupled to said input of said first latch and said output of said first latch for detecting a difference between a present state and a prior state of said output of said first differential comparator;

a second exclusive-OR gate having inputs coupled to said input of said second latch and said output of said second latch for detecting a difference between a present state and a prior state of said output of said second differential comparator; and

a third exclusive-OR gate having inputs coupled to an output of said first exclusive-OR gate and an output of said second exclusive-OR gate, and having an output coupled to a select input of said multiplexer, for

performing said selecting.

12. The interface of Claim 11, further comprising a fourth exclusive-OR gate having inputs coupled to said input of said third latch and said output of said third latch for detecting a difference between a present state and a prior state of said output of said third differential comparator, and wherein said fourth exclusive-OR gate has an output coupled to an input of said third exclusive-OR gate.

13. A receiver for receiving a differential data signal pair and a single-ended data signal, comprising:

a differential comparator coupled to said differential data signal pair; and

a singlential comparator coupled to said differential comparator and further coupled to said differential data signal pair and said single-ended data signal;

a multiplexer having an output for producing a data output signal corresponding to said single-ended data signal, having a first input coupled to an output of said differential comparator, a second input coupled to an inverted output of said differential comparator;

a first latch coupling said differential comparator to said multiplexer, said first latch having an input coupled to said output of said differential comparator and an output coupled to said first input of said multiplexer;

an inverter having an input coupled to said output of said first latch for producing said inverted output of said differential comparator and having an output coupled to said multiplexer;

a second latch for latching said output of said singlential comparator; and

an exclusive-OR gate having a first input coupled to said output of said first latch and a second input coupled to an output of said second latch and an output coupled to a select input of said multiplexer for selecting said output of said first latch when said single-ended signal

is at an equal logic value with said differential signal pair and for selecting said output of said inverter when said single-ended signal and said differential data signal pair are at unequal logic levels.

14. A receiver for receiving a differential data signal pair and a single-ended data signal, comprising:

a first differential comparator coupled to said differential data signal pair;

a second differential comparator coupled to a non-inverted signal of said differential signal pair and said single ended-data signal;

a third differential comparator coupled to an inverted signal of said differential signal pair and said single ended data signal;

a multiplexer for producing a data output corresponding to said logic value of said single-ended data signal;

a first latch having an input coupled to an output of said first differential comparator;

a second latch having an input coupled to an output of said second differential comparator and an output coupled to a first input of said multiplexer;

a third latch having an input coupled to an output of said third differential comparator and an output coupled to a second input of said multiplexer;

a first exclusive-OR gate having inputs coupled to said input of said first latch and said output of said first latch for detecting a difference between a present state and a prior state of said output of said first differential comparator;

a second exclusive-OR gate having inputs coupled to said input of said second latch and said output of said second latch for detecting a difference between a present state and a prior state of said output of said second differential comparator; and

a third exclusive-OR gate having inputs coupled to an output of said first exclusive-OR gate and an output of said second exclusive-OR gate, and having an output coupled to a select input of said multiplexer, for performing said selecting.

15. The receiver of Claim 14, further comprising a fourth exclusive-OR gate having inputs coupled to said input of said third latch and said output of said third latch for detecting a difference between a present state and a prior state of said output of said third differential comparator, and wherein said fourth exclusive-OR gate has an output coupled to an input of said third exclusive-OR gate.

16. A comparator circuit having differential inputs for receiving a differential signal pair and a single-ended input for receiving a single-ended signal, comprising:

a first transistor having a gate coupled to said single-ended signal ;

a second transistor having a gate coupled to a non-inverted signal of said differential signal pair;

a third transistor having a gate coupled to an inverted signal of said differential signal pair; and

a current source coupled to a channel connection of said first transistor, a channel connection of said second transistor and a channel connection of said third transistor, whereby said comparator detects a difference between said single-ended signal and an average of said non-inverted signal and said inverted signal of said differential signal pair.

17. The comparator circuit of Claim 16, further comprising:

a fourth transistor having a gate coupled to said non-inverted signal of said differential signal pair; and

a fifth transistor having a gate coupled to said inverted signal of said differential signal pair and a first channel connection coupled to a resistor for providing active mode operation; and

a current source coupled to a channel connection of said fourth transistor and a second channel connection of said fifth transistor, whereby said differential comparator detects a difference between said said non-inverted signal and said inverted signal of said differential signal pair, and wherein a gain of said active mode of said differential comparator is equal to a a gain of said singlential comparator.

18. A method for signaling over an electronic interface, said method comprising:

transmitting a differential data signal pair;

second transmitting a single-ended data signal;

receiving said differential data signal pair; and

detecting said single-ended data signal in conformity with a common-mode voltage of said received differential data signal pair.

19. The method of Claim 18, wherein said detecting comprises:

deriving a reference from said differential pair of data signals; and

second detecting a difference between said single-ended data signal and said derived reference.

20. The method of Claim 19, wherein said deriving is comprises summing currents proportional to a non-inverting signal of said differential data signal pair and an inverting signal of said differential data signal pair, and wherein said second detecting is comprises balancing a current proportional to said single ended data signal against said summed currents.

21. The method of Claim 18, wherein said detecting comprises:

first comparing a non-inverting signal of said differential pair to an inverting signal of said differential pair;

second comparing said single-ended data signal to said non-inverting signal of said differential data signal pair;

third comparing said single-ended data signal to said inverting signal of said differential data signal pair; and

selecting between a result of said second comparing and said third comparing, in conformity with a result of said first comparing and said second comparing.

22. The method of Claim 21, wherein said selecting is further performed in conformity with a result of said third comparing.